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10/575,042	11/13/2006	Kenichi Adachi	545/71	5950

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EXAMINER	
CHEW, BRIAN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,042	ADACHI ET AL.	
	Examiner	Art Unit	
	BRIAN CHEW	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/4/2009, 1/2/2008, 10/12/2007, 9/17/2007, 2/12/2007, 5/22/2006, 4/5/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

Claim Objections

2. Claim 4 is objected to because of the following informalities:

i. As per claim 4: Line 4: There appears to be a typographical error at "task s". This shall be amended to read -- tasks --. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** Language in the following claims is not clearly understood:

i. As per claim 1: Line 4: It is uncertain what is meant by "as appropriate" (i.e., does this refer to skipping execution of a non-real-time task so a real-time task does not miss its deadline?).

ii. As per claims 2-3, they are dependent on claim 1 but do not overcome the deficiencies of claim 1; therefore, they are rejected for the same reasons.

iii. As per claim 4:

Line 5: It is uncertain what is meant by "as appropriate" (i.e., does this refer to "if there is a possibility that real-timeness of processing is impaired by a predetermined factor"?).

Lines 5-6: It is uncertain whether "real-timeness of processing" correlates to "tasks to be executed by a processor" (i.e., what is being processed?).

iv. As per claim 5, it is dependent on claim 4 but does not overcome the deficiencies of claim 4; therefore, it is rejected for the same reasons.

v. As per claim 6:

Line 3: It is uncertain whether the "main processing unit" is part of the claimed "task management device".

Line 7: It is uncertain what is meant by "as appropriate" (i.e., does this refer to skipping execution of a non-real-time task so a real-time task does not miss its deadline?).

vi. As per claim 8: Lines 2-3: It is uncertain what is meant by "interprets a requirement pertaining to real-timeness written in programs executed by the

respective tasks" (i.e., does this mean the interpretation unit determines whether tasks require real-time processing or not?).

vii. As per claim 9: lines 2-3: There is insufficient antecedent basis for "the programs executed by the respective tasks"; Applicant is advised to amend this to read -- programs executed by the respective tasks --.

viii. As per claim 10: Lines 1-2: it is uncertain what is meant by "wherein the unit time is one pertaining to display" (i.e., does this mean the unit time is allocated to tasks for displaying?).

ix. As per claim 11: Lines 1-2: It is uncertain what the difference is between "throughput of the processor" and "usage rate of the processor" (i.e., does the throughput correspond to operating frequency and usage rate correspond to number of frames?).

x. As per claims 7 and 12, they are dependent on claim 6 but do not overcome the deficiencies of claim 6; therefore, they are rejected for the same reasons.

xi. As per claims 13 and 25, they have the same deficiencies as stated in the rejection of claim 4; therefore, they are rejected for the same reasons.

xii. As per claim 14, 24 and 26, they have the same deficiencies as stated in the rejection of claim 1; therefore, they are rejected for the same reasons.

xiii. As per claims 15-19, they are dependent on claim 14 but do not overcome the deficiencies of claim 14; therefore, they are rejected for the same reasons.

xiv. As per claim 20:

Line 5-9: It is uncertain what is claimed (i.e., are the "circuit" and "task management function" being claimed or are the method steps of "reading", "dividing" and "skipping" being claimed?).

Line 9: It is uncertain what is meant by "as appropriate" (i.e., does this refer to skipping execution of a non-real-time task so a real-time task does not miss its deadline? When the operating frequency falls? Both?).

xv. As per claim 21, it has the same deficiencies as stated in the rejection of claim 20; therefore, it is rejected for the same reasons.

xvi. As per claims 22-23, they are dependent on claim 21 but do not overcome the deficiencies of claim 21; therefore, they are rejected for the same reasons.

xvii. As per claims 27-28, they are dependent on claim 26 but do not overcome the deficiencies of claim 26; therefore, they are rejected for the same reasons.

xviii. As per claims 29-30, they have the same deficiencies as stated in the rejection of claim 20; therefore, they are rejected for the same reasons.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. **Claims 6-13, 24-25 and 29-30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.**

5. As per claim 6, it recites a "task management device"; however, it appears that the system would reasonably be interpreted by one of ordinary skill in the art as software, per se, failing to be tangibly embodied or include any recited hardware as part of the system. Software alone is directed to a non-statutory subject matter. Applicant is advised to amend the claims to include hardware (e.g., processor and memory) to overcome the §101 rejection.

6. As per claims 7-12 and 29-30, they are dependent on claim 6 but do not overcome the deficiencies of claim 6; therefore, they are rejected for the same reasons.

7. As per claim 13, it has the same deficiencies as stated in the rejection of claim 6; therefore, it is rejected for the same reasons.

8. As per claim 24, it recites a "program"; however, it appears that the system would reasonably be interpreted by one of ordinary skill in the art as software, per se, failing to be tangibly embodied or include any recited hardware as part of the system. Software alone is directed to a non-statutory subject matter. Applicant is advised to amend the claims to include hardware (e.g., processor and memory) to overcome the §101 rejection.

9. As per claim 25, it has the same deficiencies as stated in the rejection of claim 24; therefore, it is rejected for the same reasons.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1, 4-5, 14 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gomi et al. (US 5,794,036; hereinafter Gomi).**

11. As per claim 1; Gomi teaches a method of executing tasks comprising:

- dividing a unit time of processing in executing tasks by a processor into a reserved band for guaranteeing real-timeness and a non-reserved band not for guaranteeing real-timeness *(column 5, lines 1-20 and 51-65; processing A is real-time and processings B and C are non-real-time, real-time scheduling has higher priority than non-real-time scheduling)*; and
- skipping a task to be executed in the non-reserved band as appropriate when the processor falls in throughput *(column 5, lines 51-65; processing B and/or C are omitted during times of high load)*.

It is obvious to one of ordinary skill at the time the invention was made for skipping a task to be executed in the non-reserved band as appropriate when the processor falls in throughput because Gomi teaches omitting tasks during times of high load *(column 5, lines 51-65)*, which contemplates situations where the processor is unable to completely process all tasks in a timely manner.

12. As per claim 4, Gomi teaches a task management method comprising:

classifying tasks to be executed by a processor into a first type and a second type depending on properties thereof *(column 5, lines 1-20 and 51-65; processing A is real-time and processings B and C are non-real-time, real-time scheduling has higher priority than non-real-time scheduling)*; and

executing tasks of the first type while skipping a task of the second type to be executed between the tasks of the first type as appropriate if there is a possibility that real-timeness of processing is impaired by a predetermined factor *(column 5, lines 51-65; processing B and/or C are omitted during times of high load)*.

It is obvious to one of ordinary skill in the art at the time the invention was made for classifying tasks to be executed by a processor into a first type and a second type depending on properties thereof because Gomi teaches classifying processes into real-time tasks and those that are non-real-time and can be omitted *(column 5, lines 1-20 and 51-65)*.

13. As per claim 5, Gomi teaches the method of claim 4, wherein:

- the processor recognizes by a predetermined method that the task of the first type is one whose real-timeness must be guaranteed *(column 5, lines 3-11)*; and
- the processor recognizes by a predetermined method that the task of the second type is one whose real-timeness is not guaranteed *(column 5, lines 12-20)*.

14. As per claim 14, it is rejected for the same reasons as stated in the rejection of claim 1. Gomi further teaches a semiconductor integrated circuit comprising a main processing unit which executes predetermined tasks *(column 4, lines 35-36)*.

15. As per claims 24-25, they rejected for the same reasons as stated in the rejection of claim 1.

16. **Claims 2-3, 6-13, 15-23 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gomi in view of Saito et al. (US 5,723,998; hereinafter Saito).**

17. As per claim 2, Gomi teaches the method of claim 1, but is silent on wherein an operating frequency of the processor is lowered when the processor or a peripheral circuit thereof exceeds a predetermined threshold in temperature.

Saito teaches an operating frequency of the processor is lowered when the processor or a peripheral circuit thereof exceeds a predetermined threshold in temperature *(column 2, lines 20-26)*.

One of ordinary skill in the art at the time the invention was made would have been motivated to modify Gomi with the teachings of Saito so "the processor can be driven with a processing capacity appropriate to the operating environment" *(column 6, lines 26-28)*.

18. As per claim 3, Gomi teaches the method of claim 1, but is silent on wherein an operating frequency of the processor is lowered depending on power consumption of the processor.

Saito teaches an operating frequency of the processor is lowered depending on power consumption of the processor *(column 6, lines 61-64)*.

19. As per claim 6, Gomi in view of Saito teaches a task management device comprising:

- a switch instruction unit which issues an instruction to switch a plurality of tasks to be executed by a main processing unit *(Gomi: figure 2, periodic process 20; column 2, lines 27-34)*;
- a detection unit which detects a throughput of the processor *(Saito: column 5, lines 36-42)*; and
- wherein the switch instruction unit divides a unit time of processing into a reserved band for guaranteeing real-timeness and a non-reserved band not for guaranteeing real-timeness, and skips a task to be executed in the non-reserved band as appropriate when the main processing unit falls in throughput *(Gomi: column 5, lines 1-20 and 51-65; processing A is real-time and processings B and C are non-real-time, real-time scheduling has higher priority than non-real-time scheduling. Saito: column 6, lines 44-51)*,

20. As per claim 7, Gomi in view of Saito teaches the device of claim 6, and Saito further teaches wherein the detection unit detects an operating frequency of the main processing unit *(column 5, lines 41-42)*.

21. As per claim 8, Gomi in view of Saito teaches the device of claim 6, and Gomi further teaches further comprising

- an interpretation unit which interprets a requirement pertaining to real-timeness written in programs executed by the respective tasks *(column 5, lines 1-20; ; processing A is real-time and processings B and C are non-real-time)*, and
- wherein the switch instruction unit allocated each of the tasks to either the reserved band or the non-reserved band based on the interpretation *(column 5, lines 1-20 and 51-65; processing A is guaranteed and processing B and/or C are omitted during times of high load)*.

22. As per claim 9, Gomi in view of Saito teaches the device of claim 6, and Gomi further teaches further comprising

- a determination unit determines properties properties of the programs executed by the respective tasks *(column 5, lines 1-20; ; processing A is real-time and processings B and C are non-real-time)*, and
- wherein the switch instruction unit allocated each of the tasks to either the reserved band or the non-reserved band based on the determination *(column 5, lines 1-20 and 51-65; processing A is guaranteed and processing B and/or C are omitted during times of high load)*.

23. As per claim 10, Gomi in view of Saito teaches the device of claim 6, and Saito further teaches wherein the unit time is one pertaining to display *(column 6, line 48)*.

24. As per claim 11, Gomi in view of Saito teaches the device of claim 6, and Gomi further teaches further comprising

- a second detection unit which detects a usage rate of the main processing unit *(column 5, lines 35-37)*, and
- wherein the switch instruction unit modifies a rate of execution of a task to be executed in the non-reserved band according to the usage rate *(column 5, lines 51-65; processing A is guaranteed and processing B and/or C are omitted during times of high load)*.

25. As per claim 12, Gomi in view of Saito teaches the device of claim 11, but is silent on further comprising a table which stores information on a throughput of the main processing unit and the rate of execution of the task to be executed in the non-reserved band at the throughput in association with each other, and wherein when the usage rate of the main processing unit is lower than a predetermined threshold, the switch instruction unit makes the rate of execution of the task to be executed in the non-reserved band higher than the rate of execution set in the table.

It is obvious to one of ordinary skill in the art at the time the invention was made for a table which stores information on a throughput of the main processing unit and the rate of execution of the task to be executed in the non-reserved band at the throughput in association with each other because Saito teaches comparing a measured throughput value with a predetermined value and setting a corresponding operational clock speed based on the comparison, which could cause tasks to be removed from

scheduling *(column 5, lines 40-54; column 6, lines 45-51)*. It is obvious for the throughput ranges, predetermined value, conditions, corresponding operational clock speeds and scheduling policies to be mapped in a table.

It is obvious to one of ordinary skill in the art at the time the invention was made for, when the usage rate of the main processing unit is lower than a predetermined threshold, the switch instruction makes the rate of execution of the task to be executed in the non-reserved band higher than the rate of execution set in the table because Gomi teaches omitting processings based on the amount of load *("In case of high load… omitting processing C. In case of higher load… omitting processings B and C", column 5, lines 51-65)*. Further, Saito teaches rescheduling to remove a low priority task in the event temperature rises and the processing capacity decreases *(column 6, lines 45-51)*. It is obvious that although Saito teaches removing tasks based on the measure throughput, Gomi also makes adjustments to scheduling based on load. Thus, it is obvious for the load adjustment to make the rate of execution higher than that set in the table during times of low load.

26. As per claim 13, Gomi in view of Saito teaches a task management device comprising:

- a switch instruction unit which issues an instruction to switch a plurality of tasks to be executed by a main processing unit *(Gomi: figure 2, periodic process 20; column 2, lines 27-34)*; and

- a detection unit which detects a throughput of the main processing unit *(Saito: column 5, lines 36-42)*,
- wherein the switch instruction unit classifies the tasks to be executed by the main processing unit into a first type and a second type depending on properties thereof, and executes tasks of the first type while skipping a task of the second type to be executed between the tasks of the first type as appropriate if there is a possibility that real-timeness of processing is impaired by a predetermined factor *(Gomi: column 5, lines 1-20 and 51-65; processing A is real-time and processings B and C are non-real-time, real-time scheduling has higher priority than non-real-time scheduling and non-real-time tasks can be omitted)*.

27. As per claim 15, Gomi circuit of claim 14, but is silent on further comprising a clock generation unit which supplies a clock having a predetermined operating frequency to the main processing unit, and wherein the task management device skips a task to be executing in the non-reserved band as appropriate when the operating frequency falls.

Saito teaches

- a clock generation unit which supplies a clock having a predetermined operating frequency to the main processing unit *(column 5, lines 44-54)*, and
- wherein the task management device skips a task to be executing in the non-reserved band as appropriate when the operating frequency falls *(column 6, lines 45-51)*.

28. As per claims 16-17, they are rejected for the same reasons as stated in the rejection of claims 2-3.

29. As per claim 18, Gomi in view of Saito teaches the circuit of claim 15, and Saito further teaches wherein the task management unit skips the task to be executed in the non-reserved band as appropriate when the main processing unit or a periphery thereof exceeds a predetermined threshold in temperature *(column 6, lines 45-51)*.

30. As per claim 19, Gomi in view of Saito teaches the circuit of claim 15, and Saito further teaches wherein the task management unit skips the task to be executed in the non-reserved band as appropriate depending on power consumption *(column 6, lines 45-51 and 61-64; power consumption can cause operating frequency to decrease, which can cause low priority tasks to be skipped)*.

31. As per claim 20, Gomi in view of Saito teaches a semiconductor integrated circuit comprising:

- a main processing unit which executes tasks at a predetermined operating frequency *(Saito: column 5, lines 35-54)*;
- a clock generation unit which supplies a clock having the operating frequency to the main processing unit *(Saito: column 5, lines 44-54)*; and

- a circuit which realizes a task management function dynamically by reading a program for realizing the task management function from exterior *(Gomi: column 4, lines 48-54)*, wherein
- the task management function includes dividing a unit time of processing into a reserved band for guaranteeing real-timeness and a non-reserved band not for guaranteeing real-timeness, and skipping a task to be executed in the non-reserved band as appropriate when the operating frequency falls *(Gomi: column 5, lines 1-20 and 51-65; processing A is real-time and processings B and C are non-real-time, real-time scheduling has higher priority than non-real-time scheduling. Saito: column 6, lines 44-51)*.

32. As per claims 21, it is rejected for the same reasons as stated in the rejection of claim 20.

33. As per claims 22-23, they are rejected for the same reasons as stated in the rejection of claims 2-3.

34. As per claims 26, it is rejected for the same reasons as stated in the rejection of claim 20. Gomi further teaches a switch instruction unit which issues an instruction to switch a plurality of tasks to be executed by said processor *(figure 2, periodic process 20; column 2, lines 27-34)*.

35. As per claims 27-28, they are rejected for the same reasons as stated in the rejection of claims 2-3.

36. As per claims 29 and 30, they are rejected for the same reasons as stated in the rejection of claim 11.

Conclusion

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nakajima et al. (US 5,394,548) teaches delayed scheduling of non-deterministic tasks so that deterministic tasks can meet their respective deadlines.

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRIAN CHEW whose telephone number is (571)270-5571. The examiner can normally be reached on Monday-Thursday, 8:00AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Li B. Zhen/
Primary Examiner, Art Unit 2194

/B. C./
Examiner, Art Unit 2195